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METHOD AND APPARATUS FOR CONTROLLING RIPPLING DURING OPTICAL PROXIMITY CORRECTION

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BACKGROUND

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Field of the Invention

The invention relates to the process of designing and fabricating semiconductor chips. More specifically, the invention relates to a method and an apparatus for controlling rippling during an optical proximity correction (OPC)

25   process, wherein the OPC process compensates for optical effects that arise during the semiconductor fabrication process.

Related Art

Recent advances in integrated circuit technology have largely been

30   accomplished by decreasing the feature size of circuit elements on a

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semiconductor chip. As the feature size of these circuit elements continues to decrease, circuit designers are forced to deal with problems that arise as a consequence of the optical lithography process that is typically used to manufacture integrated circuits. This optical lithography process begins with the

5 formation of a photoresist layer on the surface of a semiconductor wafer. A mask composed of opaque regions, which are formed of chrome, and light-transmissive clear regions, which are generally formed of quartz, is then positioned over this photo resist layer coated wafer. (Note that the term "mask" as used in this specification is meant to include the term "reticle.") Light is then shone on the

10 mask from a visible light source, an ultraviolet light source, or more generally some other type of electromagnetic radiation together with suitably adapted masks and lithography equipment.

This light is reduced and focused through an optical system that contains a number of lenses, filters and mirrors. The light passes through the clear regions of

15 the mask and exposes the underlying photoresist layer. At the same time, the light is blocked by opaque regions of the mask, leaving underlying portions of the photoresist layer unexposed.

The exposed photoresist layer is then developed, through chemical removal of either the exposed or non-exposed regions of the photoresist layer.

20 The end result is a semiconductor wafer with a photoresist layer having a desired pattern. This pattern can then be used for etching underlying regions of the wafer.

One problem that arises during the optical lithography process is "line end shortening" and "pullback". For example, the upper portion of FIG. 1 illustrates a design of a transistor with a polysilicon line 102, running from left to right, that

25 forms a gate region used to electrically couple an upper diffusion region with a lower diffusion region. The lower portion of FIG. 1 illustrates a printed image that results from the design. Note that polysilicon line 102 has been narrowed

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using optical phase shifting in order to improve the performance of the transistor by reducing the resistance through the gate region.

Also note that because of optical effects and resist pullback there is a significant amount of line end shortening. This line end shortening is due to optical effects that cause the light to expose more of the resist under a line end than under other portions of the line.

In order to compensate for line end shortening, designers often add additional features, such as "hammer heads," onto line ends (see top portion of FIG. 2). The upper portion of FIG. 2 illustrates a transistor with a polysilicon line 202, running from left to right, which forms a gate region used to electrically couple an upper diffusion region with a lower diffusion region. A hammer head 204 is included on the end of polysilicon line 202 to compensate for the line end shortening. As is illustrated in the bottom portion of FIG. 2, these additional features can effectively compensate for line end shortening in some situations.

These additional features are typically added to a layout automatically during a process known as optical proximity correction (OPC). For example, FIG. 3 illustrates line end geometry 302 (solid line) prior to OPC and the resulting corrected line end geometry 304 after OPC (dashed line). Note that the corrected line end geometry 304 includes regions with a positive edge bias in which the size of the original geometry 302 is increased, as well as regions of negative edge bias in which the size of the original geometry 302 is decreased.

During the OPC process, edges in the layout are divided into segments at dissection points. Next, the system selects an evaluation point for each segment and then produces a bias for each segment so that a simulated image of the segment matches the target image for the segment at the evaluation point. Referring to FIG. 4, biases are introduced for each segment to produce a layout represented by the dashed line. This layout produces a simulated image

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represented by the curved line. Note that this simulated image matches the target image at evaluation points 402-404. However, this simulated image has ripples which cause large critical dimension variations in between the evaluation points.

Circuit designers presently deal with rippling by manually adjusting dissection points, evaluation points and segment biases. This manual process is time-consuming and may not be applied consistently to all portions of the layout.

What is needed is a method and an apparatus that automatically controls rippling during the OPC process.

SUMMARY

One embodiment of the present invention provides a system that controls rippling caused by optical proximity correction during an optical lithography process for manufacturing an integrated circuit. During operation, the system selects an evaluation point for a given segment, wherein the given segment is located on an edge in the layout of the integrated circuit. The system also selects at least one supplemental evaluation point for the given segment. Next, the system computes a deviation from a target location for the given segment at the evaluation point. The system also computes a supplemental deviation at the supplemental evaluation point. Next, the system adjusts a bias for the given segment, if necessary, based upon the deviation at the evaluation point. The system also calculates a ripple for the given segment based upon the deviation at the evaluation point and the supplemental deviation at the supplemental evaluation point. If this ripple exceeds a threshold value, the system performs a ripple control operation.

In a variation on this embodiment, the system adjusts the bias, if necessary, and performs the ripple control operation, if necessary, for each segment that is part of the layout of the integrated circuit.

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In a variation on this embodiment, prior to selecting the evaluation point for the given segment, the system dissects edges in the layout into segments for optical proximity correction purposes.

In a variation on this embodiment, performing the ripple control operation involves performing a refinement operation. This refinement operation involves: selecting additional dissection points for the edge that cause the given segment to be divided into multiple segments; selecting additional evaluation points for the multiple segments; and selecting additional supplemental evaluation points for the multiple segments. The refinement operation also involves adjusting the bias, if necessary, and performing the ripple control operation, if necessary, for each of the multiple segments.

In a variation on this embodiment, selecting additional evaluation points involves using supplemental evaluation points as the additional evaluation points.

In a variation on this embodiment, performing the ripple control operation involves performing a regeneration operation. This regeneration operation involves changing the location of dissection points for the edge to cause the edge to be divided into a different set of segments. It also involves adjusting the bias, if necessary, and performing the ripple control operation, if necessary, for each segment in the different set of segments. Note that changing the location of the dissection points for the edge can involve swapping dissection points and evaluation points.

In a variation on this embodiment, performing the ripple control operation involves controlling the bias for the given segment so that the ripple for the given segment does not exceed the threshold value, wherein as a consequence of controlling the bias a critical dimension for the given segment may not meet specification.

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In a variation on this embodiment, computing the deviation for the given segment involves using a model-based technique for computing the deviation.

One embodiment of the present invention produces a system for controlling rippling caused by optical proximity correction during an optical lithography process used in manufacturing an integrated circuit. During operation, the system selects a first evaluation point and one or more additional evaluation points for a given segment, wherein the given segment is located on an edge in the layout of the integrated circuit. Next, the system computes a first deviation from a target location for the given segment at the first evaluation point. The system also computes a second deviation at the second evaluation point. Next, the system adjusts a bias for the given segment, if necessary, based upon multiple deviations at multiple evaluation points, including the first deviation at the first evaluation point and the second deviation at the second evaluation point.

In a variation on this embodiment, both the first evaluation point and the second evaluation point are located on the given segment.

In a variation on this embodiment, the additional evaluation points are located on the given segment or on neighboring segments.

In a variation on this embodiment, the system adjusts the bias, if necessary, for each segment that is part of the layout.

In a variation on this embodiment, the system uses a model-based technique for computing the first deviation and the second deviation.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 illustrates the line end shortening problem.

FIG. 2 illustrates the use of a hammerhead to compensate for the line end shortening problem.

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FIG. 3 illustrates a line end prior to and after optical proximity correction.

FIG. 4 illustrates the rippling problem.

FIG. 5 is a flow chart illustrating the wafer fabrication process in accordance with an embodiment of the invention.

5   FIG. 6 illustrates the process of creating a mask to be used in fabricating an integrated circuit in accordance with an embodiment of the invention.

FIG. 7 is a flowchart illustrating the optical proximity correction process with rippling control in accordance with an embodiment of the invention.

FIG. 8 illustrates a layout including supplemental evaluation points in

10   accordance with an embodiment of the invention.

FIG. 9 illustrates an optimization based on weighted critical dimension errors in accordance with an embodiment of the invention.

FIG. 10 illustrates a refinement operation in accordance with an embodiment of the invention.

15   FIG. 11 illustrates a regeneration operation in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

Wafer Fabrication Process

20   FIG. 5 is a flow chart illustrating the wafer fabrication process in accordance with an embodiment of the invention. The system starts by applying a photoresist layer to the top surface of a wafer (step 502). Next, the system bakes the photoresist layer (step 504). The system then positions a mask over the photoresist layer (step 506), and then exposes the photoresist layer through the

25   mask (step 508). Next, the system optionally bakes the wafer again (step 514) before developing the photoresist layer (step 516). Next, either a chemical etching or ion implantation step takes place (step 518) before the photoresist layer is

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removed (step 520). (Note that in the case of a lift-off process, a deposition can take place.) Finally, a new layer of material can be added and the process can be repeated for the new layer (step 522).

5   **Design Process**

FIG. 6 illustrates the process of creating a mask to be used in the wafer fabrication process described above in accordance with an embodiment of the invention. The process starts when a circuit designer produces a design 602 in VHDL, or some other hardware description language. VHDL is an acronym for
10   VHSIC Hardware Description Language. (VHSIC is a Department of Defense acronym that stands for very high-speed integrated circuits.) The VHDL standard has been codified in Institute for Electrical and Electronic Engineers (IEEE) standard 1076-1993.

Layout 602 then feeds through a layout system that performs a number of
15   functions, such as synthesis 604, placement and routing 606 and verification 608. The result is an integrated circuit (IC) layout 610, which is in the form of a hierarchical specification expressed in a format such as GDSII.

IC layout 610 then passes into OPC post-processing system 611, which performs optical proximity corrections to compensate for optical effects that arise
20   during the photolithography process.

The output of OPC post-processing system 611 is a new IC layout 618. New IC layout 618 subsequently passes into mask fabrication and inspection processes 620.

25   **Optical Proximity Correction**

FIG. 7 is a flowchart illustrating an optical proximity correction process which takes place in OPC post-processing system 611 of FIG. 6 in accordance

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with an embodiment of the invention. The process starts when the system receives a circuit layout requiring optical proximity correction (OPC) (step 702). This circuit layout can be received in a standard format, such as GDSII format, mask electronic beam exposure system (MEBES) format or some other format.

5   Next, the system receives OPC parameters for evaluating the input circuit layout (step 704). In one embodiment of the invention, the system receives OPC parameters from a user through a graphical user interface (GUI). In another embodiment, the OPC parameters are received in a data file, such as a text file or an XML file.

10   The system then dissects polygon edges in the circuit layout into OPC segments at dissection points (step 706). This is done in accordance with the OPC parameters. For example, the parameters might specify that segments are to be dissected every 120 nm, but that segments on inside corners are to be dissected every 60 nm.

15   The system then selects a given segment for evaluation (step 708). During this evaluation, the system then selects an evaluation point for the given segment (step 710).

The system also may select one or more supplemental evaluation points to be used in concert with the evaluation point to detect rippling (step 712). Note that

20   supplemental evaluation points can be selected based on a set of user-specified rules. They are typically placed at locations at which the maximum amount of potential ripple can be measured. For example, they can be placed half way between evaluation points, or at dissection points where OPC encounters abrupt changes. They can also be placed based on results of a simulation.

25   The system next calculates a critical dimension (CD) deviation at the evaluation point for given segment (step 714). This can be done by using an optical model of the lithography process at the evaluation point. The system also

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calculates a supplemental deviation at the supplemental evaluation points (step 716). Note, although steps 710 through 718 are shown in sequence, they may be performed in parallel and/or out of order as appropriate. For example, the selection and computation of deviation for the supplemental evaluation points can

5   occur on separate process threads from the computations for the evaluation point, as long as the ripple control operation is performed for the edge being considered before moving on to the next edge (before returning to step 708).

Next, the system adjusts a bias for the given segment (step 718). This bias adjustment is calculated based upon the deviation at the evaluation point.

10   Alternatively, the bias adjustment can be calculated based upon a weighted function of the deviation at the evaluation point and the deviations at one or more additional evaluation points as is described below with reference to FIG. 9.

Next, the system calculates a "ripple" for the segment (step 720). The ripple is a value that measures the variation of CD values along the segment. In

15   one embodiment of the invention, this ripple is computed by squaring the difference between the deviation at the evaluation point, d_e, and the deviation at each supplemental evaluation point, $d_{s(i)}$, and then averaging the squares to produce a positive ripple value, $\sum_{i=1}^{N} \dfrac{\left(d_e - d_{s(i)}\right)^2 w_i}{N}$, where N is the number of supplemental evaluation points, and w_i's are the constant weighting coefficients.

20   In another embodiment, the ripple may simply be the maximum difference of deviations between any evaluation or supplemental evaluation points, i.e., $\max\left\{\max_{i,j}\left|d_{s(i)} - d_{s(j)}\right|, \max_{i}\left|d_e - d_{s(i)}\right|\right\}$. The system then compares the ripple with a threshold value (step 722).

If the ripple is larger than the threshold value, the system performs a

25   refinement operation that breaks the segment into multiple segments in order to

more accurately control ripple (step 724). The threshold values are also user selected, and can be chosen to be shape dependent. For example, this threshold value can be selected based upon the edge specification and/or the critical dimension tolerance. One way to accomplish this is to select the threshold to be proportional to the critical dimension tolerance of the edge being processed. For example, if an edge has a tolerance of 5nm (i.e., printed edge can be as far as 5nm deviated from ideal), the maximum ripple should not exceed 3nm (so that at the supplemental evaluation points the deviation is at most 8nm). The refinement operation is described in more detail below with reference to FIG. 10. The system then determines if the refinement operation was successful (step 726). Note that the refinement operation may fail if the given segment is too small to be subdivided into multiple segments. If the refinement operation was successful (that is, new segments are created that replace the segments that have been refined), the system returns to step 708 to process the newly created segments as well as the remaining segments.

Otherwise, if the refinement at step 724 operation fails, the system performs a regeneration operation to change dissection points and/or evaluation points for the edge (step 728). This regeneration process is described in more detail below with reference to FIG. 11. The system then determines if the regeneration operation was successful (step 730). If so, new segments will have been created that replace the segments being regenerated, the system returns to step 708 to process the regenerated segments as well as the remaining segments.

If not, the system limits biasing of the segment in order to control the rippling (step 732). If the rippling exceeds a preset maximum threshold value, which can be determined for example based on a percentage, the system reduces the bias for the segment to stop the edge movement, even if the segment is not close enough to its target location to satisfy a design specification. The segment

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will hopefully be corrected to fall within specification in a subsequent iteration. If not, the user either has to accept this fact, or the user has to consider new dissection parameters to hopefully improve the situation. Note that the specification must sometimes be sacrificed in order to compromise with other

5   factors, such as ripple, spacing constraints, and width constraints. Note that this bias limiting technique generally reduces aggressive edge movements during optical proximity correction. For segments that remain too far from meeting specification, a new dissection may need to be generated. Next, the system the returns to step 708 to get the next segment.

10   If the ripple is smaller than the threshold value at step 722, the system determines if there are more segments to process (step 734). If not, the system proceeds to update the layout with the edge biases that have been calculated for each segment (step 736). Finally, the system determines if stopping criteria have been satisfied (step 738). If not, the system returns to step 708 for another

15   iteration. Otherwise, the system terminates the process. The stopping criteria can include, reaching a preset maximum number of iterations, all segments reaching a maximum correction, exhaustion of allowed computational time, all segments being fully corrected, some segments are determined to be non-correctable or not further correctable for certain reason (e.g., low contrast), and/or combinations of

20   one or more stopping criterion.

Note that the system may also decide to drop the evaluation of supplemental evaluation points and stop ripple control related operations (steps 712, 716, 720 – 732) for selected segments after the first few iterations, when it is determined that the segments are not subject to serious rippling effect. Doing so

25   saves the computation time related to ripple computation and control of these segments.

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Supplemental Evaluation Points

FIG. 8 illustrates a layout of a geometrical feature that includes supplemental evaluation points in accordance with an embodiment of the invention. This geometrical feature includes four dissection points 801-804,

5   shown as squares, that define three segments running between the dissection points.

A first segment between dissection points 801 and 802 includes an evaluation point 805, shown as a plus sign. Evaluation point 805 is can be located on the first segment, but may in some cases reside on a neighboring segment

10   and/or off the segment, e.g. displaced by a bias from the segment. Note that there may be more than one evaluation point for each segment. In addition to evaluation point 805, the first segment includes supplemental evaluation points 808 and 809, shown as circles with X's. Note that supplemental evaluation points 808 and 809 are generally located on the first segment or on adjacent segments.

15   For example, they may coincide with the dissection point associated with the segment. In another embodiment, the points may simply be neighboring segments' evaluation points. Also note that there may be one or more supplemental evaluation points for each segment.

Similarly, a second segment between dissection points 802 and 803

20   includes an evaluation point 806. The second segment also includes supplemental evaluation points 810 and 811.

Finally, a third segment between dissection points 803 and 804 includes an evaluation point 807. The third segment also includes supplemental evaluation points 812 and 813.

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Optimizations Based on Weighted CD Errors

FIG. 9 illustrates an optimization process based on weighted critical dimension errors in accordance with an embodiment of the invention. In this example, a segment defined by dissection points 901 and 902 includes evaluation point 903 and supplemental evaluation points 904 and 905. Evaluation point 903 has a deviation (also known as a "critical dimension error") d_e. Supplemental evaluation point 904 has a deviation d_{s1} and supplemental evaluation point 905 has a deviation d_{s2}. During the bias adjustment process described with reference to step 718 of FIG. 7, the bias adjustment can be made to minimize d_e^2. Alternatively, the bias adjustment can be made to minimize a weighted average of the deviations, such as,

$$d_e^2 + w_1 d_{s1}^2 + w_2 d_{s2}^2, \text{ or}$$
$$d_e^2 + w_1(d_{s1} - d_e)^2 + w_2(d_{s2} - d_e)^2.$$

Note that by minimizing these weighted averages instead of d_e^2, rippling is reduced.

Refinement

FIG. 10 illustrates a refinement operation in accordance with an embodiment of the invention. In this example, a dissection defined by dissection points 1001, 1002, 1008 and 1011 includes evaluation points 1003-1005 and supplemental evaluation points 1006-1007. During the refinement operation, the segment from 1008 to 1011 is subdivided into multiple sub-segments by introducing additional dissection points 1009 and 1010. In this example, supplemental evaluation points 1006-1007 are converted into evaluation points for corresponding sub-segments. The system can also select, or create, additional

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supplemental evaluation points (not shown) for the newly created segments, i.e. 1008 to 1009, 1009 to 1010, and 1010 to 1011.

Regeneration

5   FIG. 11 illustrates a regeneration operation in accordance with an embodiment of the invention. In this example, an edge 1100 is initially associated with dissection points 1101-1103 and evaluation points 1104-1106. Edge 1100 is regenerated by swapping the dissection points 1101-1103 and the evaluation points 1104-1106, shown as dashed symbols on the figure. This regeneration may

10   result in a better optical proximity correction, with less rippling effect. Note that in occasions where the regeneration results in worse rippling effect, this regeneration is undone and the regeneration is considered failed. Hence, ripple-controlled biasing (step 732 in FIG. 7) must be performed on the original dissection.

15   In the example illustrated in FIG. 11, dissection points 1101-1103 are converted into evaluation points and evaluation points 1104-1106 are converted into dissection points. However, in general, any modification of the dissection points 1101-1103 and the evaluation points 1104-1106 can be performed during a regeneration of edge 1100. The regeneration is can be based on the current ripple

20   measurement information so as to minimize rippling effect for the regenerated segments.

      The foregoing description is presented to enable one to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily

25   apparent, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the invention is not intended to be limited to the embodiments

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shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

The data structures and code described in this detailed description can be stored on a computer readable storage medium, which may be any device or

5   medium that can store code and/or data for use by a computer system. This includes, but is not limited to, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs) and DVDs (digital versatile discs or digital video discs), and computer instruction signals embodied in a transmission medium (with or without a carrier wave upon which the signals are modulated).

10   For example, the transmission medium may include a communications network, such as the Internet.

Note that the present invention can be applied to any type of lithographic process for fabricating semiconductor chips, including processes that make use of, deep-ultraviolet (DUV) radiation, extreme ultraviolet (EUV) radiation, X-rays,

15   and electron beams, along with suitably modified masks.

The foregoing descriptions of embodiments of the invention have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the invention to the forms disclosed. Accordingly, many modifications and variations will be apparent. Additionally, the above

20   disclosure is not intended to limit the invention. The scope of the invention is defined by the appended claims.

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